

## STD100N3LF3

# N-channel 30 V, 0.0045 Ω 80 A, DPAK planar STripFET™ II Power MOSFET

#### **Features**

Туре	$v_{\text{DSSS}}$	R <sub>DS(on)</sub>	I <sub>D</sub>	Pw
STD100N3LF3	30 V	$<$ 0.0055 $\Omega$	80 A <sup>(1)</sup>	110 W

- 1. Current limited by package
- 100% avalanche tested
- Logic level threshold

#### **Applications**

- Switching application
  - Automotive



This STripFET<sup>TM</sup> II Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

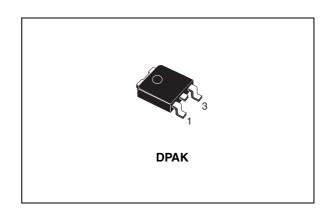


Figure 1. Internal schematic diagram

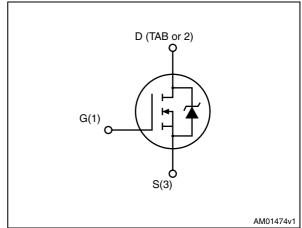


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD100N3LF3	STD100N3LF3 100N3LF3		Tape and reel

Contents STD100N3LF3

## **Contents**

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STD100N3LF3 Electrical ratings

## 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	30	V
V <sub>GS</sub>	Gate-source voltage	± 20	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	80	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> =100 °C	70	Α
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	320	Α
P <sub>TOT</sub>	Total dissipation at $T_C = 25$ °C	110	W
	Derating factor	0.73	W/°C
dv/dt (3)	Peak diode recovery voltage slope	3.9	V/ns
T <sub>stg</sub>	Storage temperature	-55 to 175	°C
$T_J$	Max. operating junction temperature	-55 to 175	

- 1. Current limited by package.
- 2. Pulse width limited by safe operating area
- 3.  $I_{SD} \le 80A$ ,  $di/dt \le 360 A/\mu s$ ,  $V_{DS} \le V_{(BR)DSS}$ ,  $T_J \le T_{JMAX}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thJC</sub>	Thermal resistance junction-case max	1.36	°C/W
R <sub>thJA</sub>	Thermal resistance junction-ambient max	100	°C/W
T <sub>I</sub>	Maximum lead temperature for soldering purpose	275	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Not-repetitive avalanche current (pulse width limited by T <sub>J</sub> max)	40	Α
E <sub>AS</sub>	Single pulsed avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AV, VDD} = 24$ V)	500	mJ

Electrical characteristics STD100N3LF3

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$I_D = 250 \ \mu\text{A}, \ V_{GS} = 0$	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating, V <sub>DS</sub> = Max rating @125 °C			1 10	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20 V			±200	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		2.5	V
		$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$ $V_{GS} = 5 \text{ V}, I_D = 20 \text{ A}$		0.0045 0.008	0.0055 0.01	Ω
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A @ 125 °C V <sub>GS</sub> = 5 V,		0.0068		Ω
		I <sub>D</sub> = 20 A @ 125 °C		0.0146		Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 10 V <sub>,</sub> I <sub>D</sub> = 15 A	-	31		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$	-	2060 728 67		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ = 24 V, $I_{D}$ = 80 A $V_{GS}$ = 5 V Figure 16 on page 9	-	20 7 7.5	27	nC nC nC
$R_{G}$	Gate input resistance	f = 1 MHz gate DC Bias = 0 test signal level = 20 mV open drain	-	1.9		Ω

<sup>1.</sup> Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$\begin{array}{c} t_{\rm d(on)} \\ t_{\rm r} \\ t_{\rm d(off)} \\ t_{\rm f} \end{array}$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD}$ = 15 V, $I_{D}$ = 40 A, $R_{G}$ =4.7 $\Omega$ , $V_{GS}$ =10 V Figure 15 on page 9	-	9 205 31 35	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I <sub>SD</sub>	Source-drain current		-		80	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		320	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 40 A, V <sub>GS</sub> = 0	-		1.3	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 80 \text{ A},$ di/dt = 100 A/ $\mu$ s, $V_{DD} = 25 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$ Figure 17 on page 9	-	40 40 2		ns µC A

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: pulse duration=300µs, duty cycle 1.5%

Electrical characteristics STD100N3LF3

#### 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

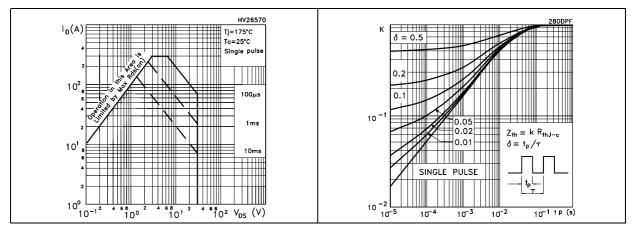


Figure 4. Output characteristics

Figure 5. Transfer characteristics

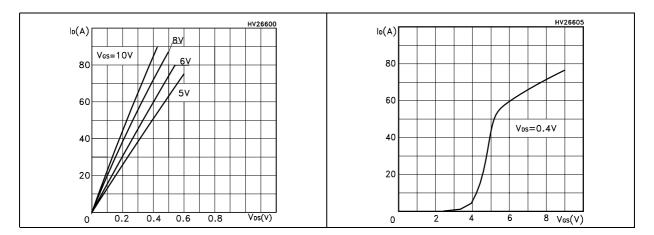


Figure 6. Transconductance

Figure 7. Static drain-source on resistance

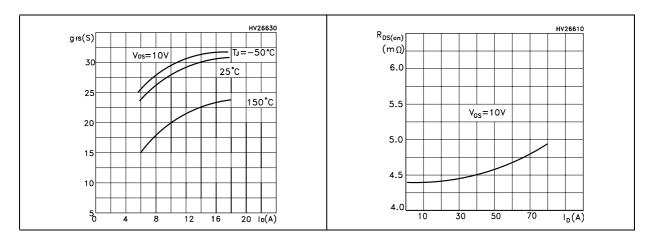


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

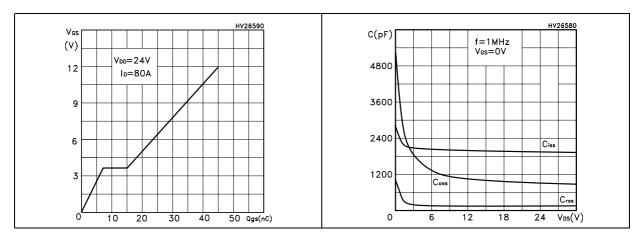


Figure 10. Normalized gate threshold voltage Figure 11. Normalized BV<sub>DSS</sub> vs temperature vs temperature

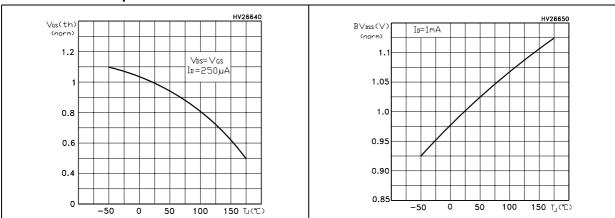


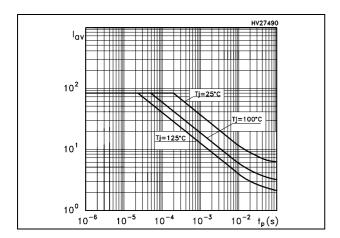
Figure 12. Normalized on resistance vs temperature

HV26620 HV26660 VsD Ros(on) (norm) 1.1 2.2 TJ=-50℃ 1.0 25°C 0.9 1.4 175℃ V<sub>G</sub>s= 10V 1.0 0.8 0.6 0.7 0.6L 0 100 -50 0 50 150 TJ(℃) 30 60 90 (A)dzI

Figure 13. Source-drain diode forward characteristics

Electrical characteristics STD100N3LF3

Figure 14. Allowable lav vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

I<sub>AV</sub> is the allowable current in avalanche

 $P_{D(AVE)}$  is the average power dissipation in avalanche (single pulse)

t<sub>AV</sub> is the time in avalanche

STD100N3LF3 Test circuits

### 3 Test circuits

Figure 15. Switching times test circuit for resistive load

Figure 16. Gate charge test circuit

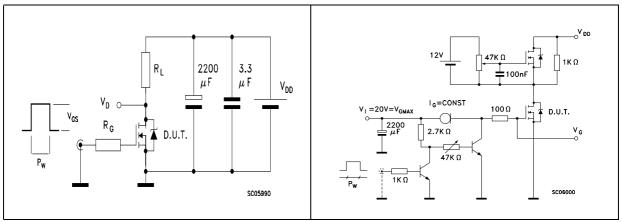
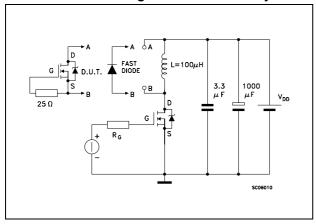


Figure 17. Test circuit for inductive load switching and diode recovery times



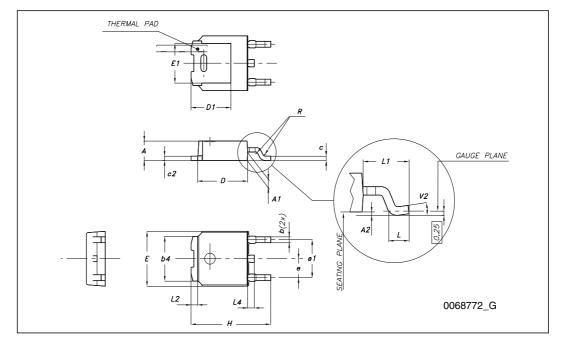
# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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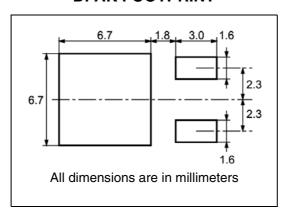
#### TO-252 (DPAK) mechanical data

DIM.	mm.		
DIWI.	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
е		2.28	
e1	4.40		4.60
Н	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °

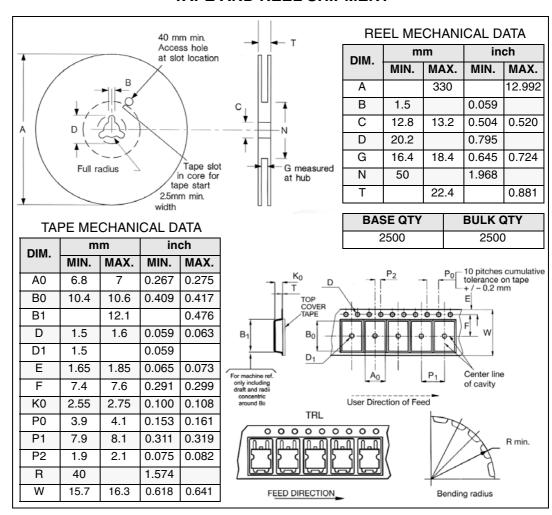


### 5 Packaging mechanical data

#### **DPAK FOOTPRINT**



#### TAPE AND REEL SHIPMENT



STD100N3LF3 Revision history

# 6 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Feb-2006	1	Initial release.
07-May-2009	2	Added V <sub>GS(th)</sub> max value in <i>Table 5: On/off states</i>
09-Nov-2009	3	Added V <sub>GS</sub> parameter in <i>Table 2: Absolute maximum ratings</i>

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